

# A Bio-amplifier with Pulse Output

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**Abstract**—A low-power fully integrated bioamplifier is presented that can amplify signals in the range from mHz to kHz while rejecting large DC offsets generated at the electrode-tissue interface. The novel aspect of this amplifier is that its analog output is represented by a series of pulses which provide a low-power, noise-resistant means for coding and transmission. The original analog signal can be reconstructed from the resulting pulse train with 13 bit precision at a remote site where power consumption is not so crucial. The fabricated analog amplifier exhibits a gain of 39.5dB from 0.3 Hz to 5.4k Hz. The power consumption of the whole system is less than 300  $\mu$ W/channel from a 5-V supply. The fully integrated system was designed in the AMI 0.6 $\mu$ m CMOS process and it consumes 0.088 mm<sup>2</sup>/channel of chip area.

**Keywords:** Bio-amplifier, CMOS, low power, pulse train

## I. INTRODUCTION

The steady advance in MEMS technology has stimulated the rapid growth of electrode array micro-sensors used in biomedical applications, especially in the field of neural recording [1]. Implanted electrodes in sub-cortical regions are used to investigate the correlation between neuron population activity and associated subject behavior. Hardware for recording the signal directly from the electrodes must be small and low power to satisfy the implantation requirements for a large number of channels. One of the solutions is to use CMOS circuits to acquire and process the electrical signals transduced from implanted extracellular cortical electrodes.

The extracellular neural signals have amplitudes of 50-500 $\mu$ V [2], but large DC offsets arise across different recording electrodes due to electrochemical effects at the electrode-tissue interface. The magnitude of these DC offsets is about 1-2V [3], much larger than the neural signals to be measured. The frequencies of the brain waves range from 100Hz to 7kHz [4], while the Local Field Potentials (LFP) extend to below 1Hz. Thus, the ideal band-pass filter for neural recording must reject the DC offset while passing the LFP signal.

Although the recording signal is analog, post-processing algorithms are more and more digitally based, which raises the need of translating the analog signals to digital representations through analog to digital converters (ADC) [4]. An on-chip ADC is required to enhance signal-to-noise ratio, increase robustness and provide a wireless transmission interface to reduce the risk of infection for chronic recording [5], [7], [6].

In the proposed circuitry, the analog output of the amplifier is translated to a series of asynchronous pulses which has better noise immunity than conventional analog signals in transmission and also eliminates the need for a traditional ADC. We have shown mathematically that the original

bandlimited signal can be perfectly reconstructed solely from noise-free pulse timings. The pulse representation strategy tradeoffs a simpler, lower-power circuit with a more complicated signal reconstruction algorithm which is presumably run outside the body where power consumption is not such a critical resource.

## II. CIRCUIT DESIGN

Fig. 1 shows the block diagram of the on-chip circuitry. Due to the very small input signal amplitude, it is necessary to preamplify the signal prior to other processing. The first stage is a pre-amplifier providing about 40dB gain at the passband and an AC coupling technique is used to reject the inherent DC offset. The second stage is an integrate-and-fire neuron which encodes the analog information in a pulse train. The voltage output of the amplifier is first converted into current and, by integrating this current, the amplitude information is encoded into an asynchronous digital pulse train.

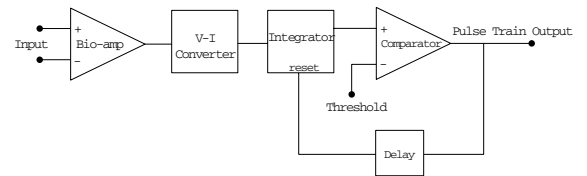


Fig. 1. Block diagram of the on-chip circuitry

### A. Preamplifier

The structure of the preamplifier was originally proposed by Harrison in [8]. Fig. 2 shows the schematic of the bio-amplifier. The midband gain  $A_m$  is  $C_1/C_2$ , the bandwidth is approximately  $g_m/(A_m C_L)$ , where  $g_m$  is the transconductance of the operational transconductance amplifier (OTA).

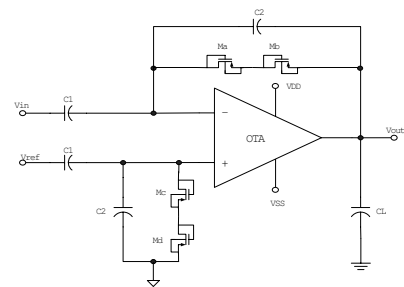


Fig. 2. Schematic of bio-amplifier

1) *Pseudo-Resistor Element*: The four diode-connected PMOS transistors  $M_a \sim M_d$  in Fig. 2 act as a “pseudo-resistor.” The pseudo-resistor functions as a pair of diodes in parallel, with opposite polarity. The current increases exponentially with voltage for either sign of voltage, and there is an extremely high resistance region around the origin. For  $|\Delta V| < 0.2V$ , we measured  $dV/dI > 10^{11}\Omega$ . The I-V relationship of the pseudo-resistor shows that the effective resistance is huge for small signals and small for large signals as shown in Fig. 3. We use two pseudo resistors in series to provide a larger voltage range. The lower cutoff frequency  $\omega_L$  is approximately  $1/(2r_p C_2)$ .

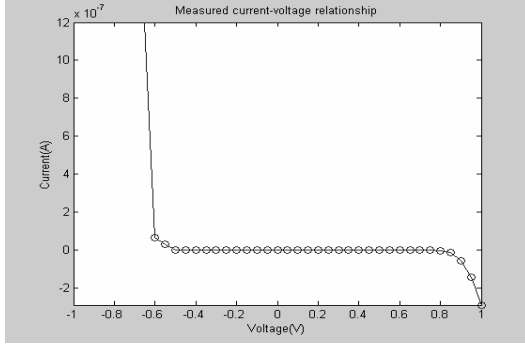


Fig. 3. Measured I-V curve of pseudo resistor

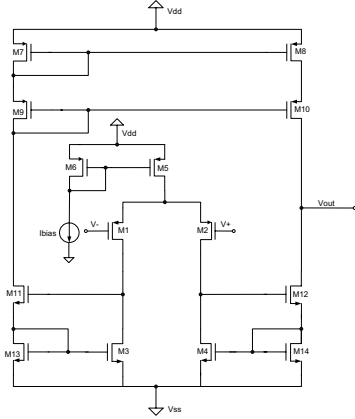


Fig. 4. Operation transconductance amplifier

2) *OTA Design*: Fig. 4 shows the schematic of the OTA used in the bio-amplifier. The OTA is a typical two stage CMOS amplifier with a P-type input differential pair for lower flicker noise [9]. The circuit operates from a 5V power supply. The input differential pair  $M_1/M_2$  is actively loaded by Wilson current mirrors.

### B. Voltage to current conversion and pulse generator

Compared with analog signals, digital signals are much more robust to transmit. Digital signals are easily storable and can be processed by powerful digital algorithms. The most popular class of A/D converter is the Nyquist-Rate converter

which can be loosely defined as those converters that generate a series of output values in which each value has a one-to-one correspondence to a single input value. The resolution of the Nyquist-Rate converter is limited by the power supply. Scaling to submicron technologies, this high resolution analog circuit is complicated by low-power supply and poor transistor output resistance (caused by the body-effect). One solution to this limitation is to employ  $\Delta-\Sigma$  A/D converter which relaxes the requirement on the analog circuitry at the expense of more complicated digital circuitry.

In this paper, our approach is to employ an integrate-and-fire asynchronous mechanism. As Fig. 5 shows, the voltage output of the amplifier is linearly converted to current by dropping the voltage across a fixed resistor  $R$ .  $V_{ref-supply}$  is used to adjust the DC shift of current. Since the following stage only deals with one sign of current, the  $V_{ref-supply}$  should be less than  $V_{mid-b}A_m$ , where  $b$  is the maximum input signal. This current charges  $C_i$  until the voltage across the capacitor reaches a fixed voltage threshold  $V_{th}$ , then the comparator output turns to high. The high voltage opens switch  $M_5$  and quickly pulls the positive node of the comparator down to ground, the output of comparator goes down correspondingly, thus generating a pulse. The width of the pulse is decided by the speed of the comparator and the time delay of the buffer.

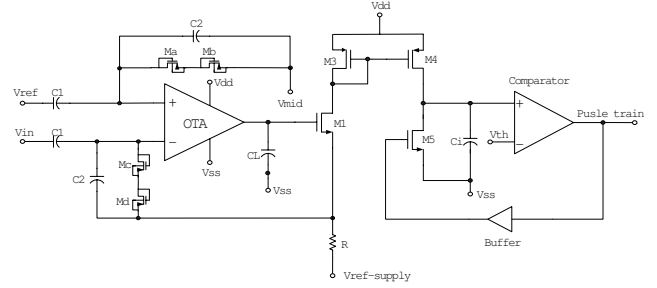


Fig. 5. Schematic of bio-amplifier with pulse output

The interval between two adjacent pulses represents the charging time, i.e. the integrating time. The following equations describe the relationship between the interval of two consecutive pulses and the input:

$$v_{out,amp} = A_M v_{in} \quad (1)$$

where  $A_M$  is the midband gain of the bio-amplifier;  $M_1$  works as a voltage follower. The AC signal at the source of  $M_1$  approximately equals the output of the bio-amplifier.

$$i_i = v_{out,amp}/R = A_M v_{in}/R \quad (2)$$

$$\int_{t_k}^{t_{k+1}} [i_i + (V_{mid} - V_{ref-supply})/R]/C_i dt = V_{th} \quad (3)$$

Substituting Eq. 2 into Eq. 3 yields

$$\int_{t_k}^{t_{k+1}} [v_{in} A_M - V_{ref-supply} + V_{mid}] dt = V_{th} C_i R \quad (4)$$

If the input signal is bounded by a constant  $b$  and band-limited to  $\Omega$ . The lower and upper bounds on the distance between two consecutive pulses  $t_k$  and  $t_{k+1}$  is given by:

$$t_{k+1} - t_k \geq \frac{C_i R V_{th}}{V_{mid} - V_{ref-supply} + bA_m} \quad (5)$$

$$t_{k+1} - t_k \leq \frac{C_i R V_{th}}{V_{mid} - V_{ref-supply} - bA_m} \quad (6)$$

According to the results in [10] and [11], if  $\Delta t_{max} < \frac{\pi}{\Omega}$ , the original analog signal can be recovered perfectly. By carefully choosing  $V_{ref-supply}$ ,  $V_{th}$ ,  $C_i$ , and  $R$ , we can reconstruct the input analog signal using only the timing information of the pulse train output.

### C. Power Budget

Power consumption is a major concern for many biomedical circuits. There are three major subcircuits to consider in computing the total power: 1) the bio-amplifier and comparator, 2) the V-I converter and 3) the delay circuit. The power consumption of the bio-amplifier and comparator is determined by the bias currents. The power consumption of the V-I converter is:  $P_{V-I} = I_{rms} V_{DD}$  where  $I_{rms}$  is the current across  $R$ . Since the input signal is bounded, an upper bound for  $P_{V-I}$  is

$$P_{V-I} < \frac{(V_{mid} - V_{ref-supply} + bA_m)V_{DD}}{R} \quad (7)$$

The delay circuit uses two digital CMOS inverters to produce the delay from the output of the comparator to the integrator. The average power consumption in conventional CMOS digital circuits can be expressed as the sum of three main factors: the dynamic (switching) power consumption, the short-circuit power consumption, and the leakage power consumption [12]. The first component represents the power dissipated during a switching event. The average power dissipation of the CMOS logic gate can be calculated from the energy required to charge up the output node to  $V_{DD}$  and discharge the output load capacitance to ground [12]:

$$P_{avg} = C_{load} V_{DD}^2 f \quad (8)$$

where  $C_{load}$  is the load capacitance the inverters drive;  $f$  is the switching frequency of the inverters. For the pulse generator, the switching speed is determined by the input. If the input is bounded by a constant  $b$ , the highest switching frequency is:

$$f_{p,max} = \frac{V_{mid} - V_{ref-supply} + bA_m}{V_{th} R C_i} \quad (9)$$

The average dynamic power dissipation is bounded by:

$$P_{avg}(dynamic) < C_{load} V_{DD}^2 f_{p,max} \quad (10)$$

The power dissipation caused by the current when nMOS and pMOS transistors are open simultaneously is called short-circuit power dissipation. For simplicity, assume  $\kappa_n = \kappa_p = \kappa$ ,  $V_{T,n} = V_{T,p} = V_T$  and equal rise and fall time ( $\tau_{rise} = \tau_{fall} = \tau$ ):

$$P_{avg}(short - current) < \frac{1}{12} \kappa \tau f_{p,max} (V_{DD} - 2V_T)^3 \quad (11)$$

TABLE I  
THE MEASURED CHARACTERISTICS OF BIO-AMPLIFIER

Parameter	Measured results
Supply voltage	5V
Supply current	8 $\mu$ A
Gain	39.5dB
Bandwidth	5.4K Hz
Lower cutoff frequency	$\sim$ 0.3 Hz
Input referred noise	9.56 $\mu$ V $_{rms}$
CMRR	$\sim$ 59.2dB
PSRR	$\sim$ 45dB

Since there are only 5 transistors used in this part of the circuit, the leakage power dissipation caused by reverse leakage and subthreshold current in our design is negligible. Thus, the total power dissipation caused by the delay is approximately:

$$P_{avg}(delay) \simeq P_{avg}(dynamic) + P_{avg}(short - current) \quad (12)$$

### D. Reconstruction methodology

According to Eq. 3, the analog information is encoded into the timing difference between two adjacent pulses. We can define the timing of pulses:  $\mathbf{T}=[t_1, t_2, \dots, t_k, t_{k+1}, \dots]$ . Let  $x(t) = v_{in} A_m - V_{ref-supply} + V_{mid}$  and  $s_k = (t_{k+1} + t_k)/2$ . Theories proposed in [11] show that we can recover the original input signal from the timing information: Define  $\mathbf{g}=[g(t - s_k)]^T$ ,  $\mathbf{q}=[\int_{t_k}^{t_{k+1}} x(u) du]$  and  $\mathbf{G}=[\int_{t_j}^{t_{j+1}} g(u - s_k) du]$ , where  $g(t) = \sin(\Omega t)/\pi t$ , the  $x(t)$  can be perfectly recovered from  $\mathbf{T}$  as

$$x(t) = \mathbf{g} \mathbf{G}^+ \mathbf{q} \quad (13)$$

where  $\mathbf{G}^+$  denotes the pseudo-inverse of  $\mathbf{G}$ .

## III. EXPERIMENTAL RESULTS

We fabricated the circuitry in the AMI 0.6 $\mu$ m three-metal two-poly process. The designed amplifier gain is 40dB. Using poly-to-poly capacitors, we set  $C_2$  to 200fF,  $C_1$  to 20pF,  $C_L$  to 6pF and  $C_i$  to 10pF. The resistance value of  $R$  is set to 15K $\Omega$  and built with a long poly wire.

### A. Preamplifier

We used the signal analyzer from Audio Precision Inc. to measure the analog specifications. Fig. 6 shows the frequency response. The measured midband gain is 39.5 dB and high cutoff frequency is 5.4KHz. Since the lowest frequency this instrument can measure is 10 Hz, the low cutoff frequency was measured by adjusting the frequency of single sine wave input and observing the output of the amplifier. The measured lower cutoff frequency is around 0.3 Hz. Other specifications are shown in Table I.

### B. Pulse output and reconstruction

We used an Agilent 1693 digital analyzer to record the timing information of the pulse output with the sample rate of 5ns. When the bias current of the comparator was 0.3 $\mu$ A, the average pulse width was 108.24ns with a standard deviation of 2.39ns. As IEEE-STD-1241 requires, a curve fitting method

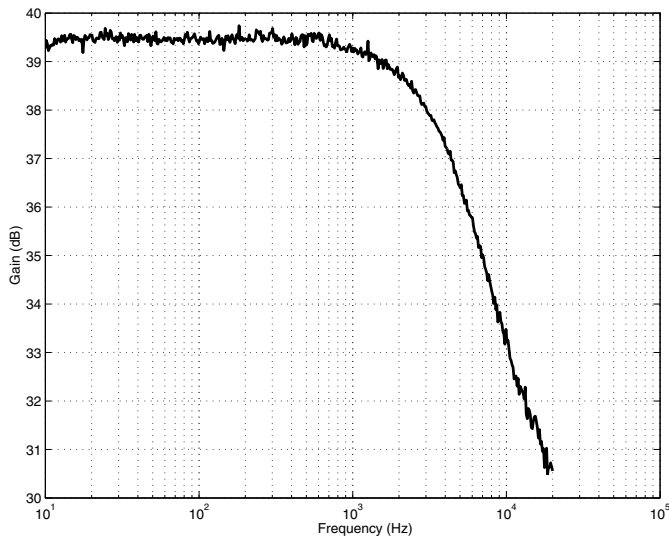


Fig. 6. Measured frequency response of the bio-amplifier

(sine wave fitting) was used to evaluate the reconstruction performance. There are 4 basic steps to characterize an ADC [14]: 1) set up the device; 2) apply a single tone sine wave as an input; 3) collect sampled and quantized data; and 4) calculate standardized parameters using off-line algorithms. The input is a 2mV 1kHz sine wave. The off-line algorithm we use is an ADC test evaluation program [13], which determines that the reconstructed sine wave has 13 effective bits. Fig. 7 shows the recorded pulse train and reconstructed sine wave.

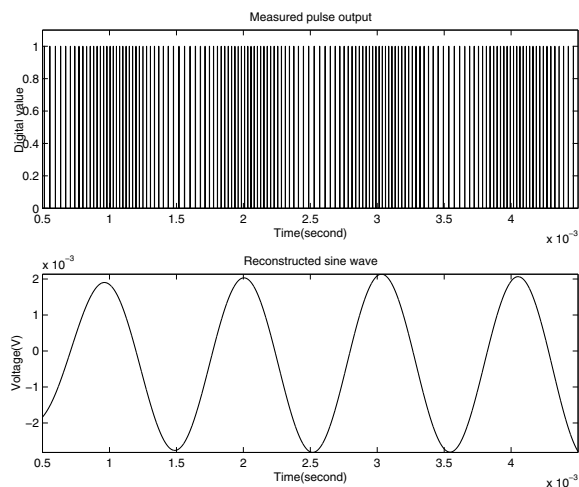


Fig. 7. Measured pulse output and reconstructed signal

#### IV. CONCLUSIONS

A fully-integrated CMOS bio-amplifier with pulse output has been demonstrated. The system allows recording of the neural signals down to tens of  $\mu\text{V}$ . These signals are amplified using a fully integrated preamplifier with 39.5dB gain. The amplifier can reject DC drift introduced at the electrode and electrolyte interface, but still pass low frequency signal down

to the mHz range without using any off-chip capacitors. Furthermore, the amplified analog signals are sampled by a integrate-and-fire asynchronous pulse generator. By using the timing information between pulses, the original analog signal can be reconstructed with 13 effective bits. The circuit is designed with a CMOS process. The power dissipation of whole system is less than  $300\mu\text{W}/\text{channel}$  from a 5-V supply and consumes  $0.088\text{ mm}^2$  of area.

Since the integrate-and-fire mechanism does not operate on signals with both positive and negative values, the proposed circuit uses a DC shift to rectify the signal. This DC shift results in higher firing rate and greater power dissipation. With a simple modification to the existing architecture, the DC shift can be eliminated by employing two integrate-and-fire circuits that encode positive and negative signals respectively.

This asynchronous pulse train representation implements a novel tradeoff: a simpler analog design at the frontend vs. a more complex digital reconstruction process at the backend. Such a tradeoff is well suited for low-power implanted bioinstrumentation systems, as well as many other applications dealing with distributed sensing.

#### V. ACKNOWLEDGMENT

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