EEL6935 – Fall 2003
HW #3 Due October 15, 2003

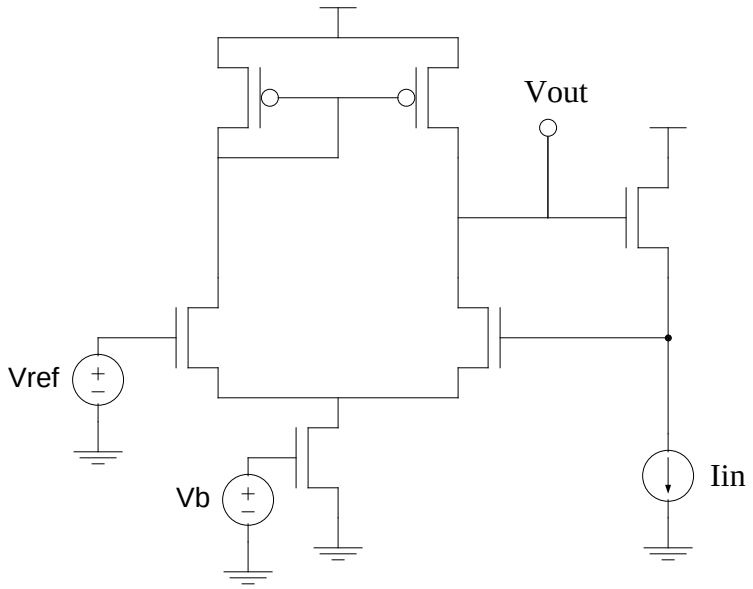
NAME: _____

Due Wednesday, October 15, 2002 in class. Late homework loses $e^{\#\ of\ days\ late} - 1$ percentage points. See the current late penalty at
http://www.cnel.ufl.edu/hybrid/harris/latepoints.html This exam has been designed to get you ready for our exam on October 22, periods E1-E2. You need to hand back this homework written only on these pages. You can print out another copy of this pdf file from the website if you want to start over.

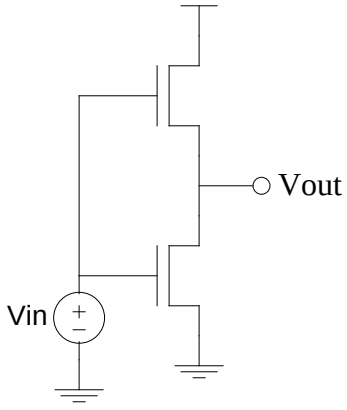
The instructions for the exam will be something like the following:
This exam is open-book and calculator. You may use any books or papers that you like. There are four problems on this exam, you have two full class periods. State your assumptions and reasoning for each problem. Justify your steps and clearly indicate your final answers.

1	**/25**
2	**/25**
3	**/25**
4	**/25**
TOTAL	

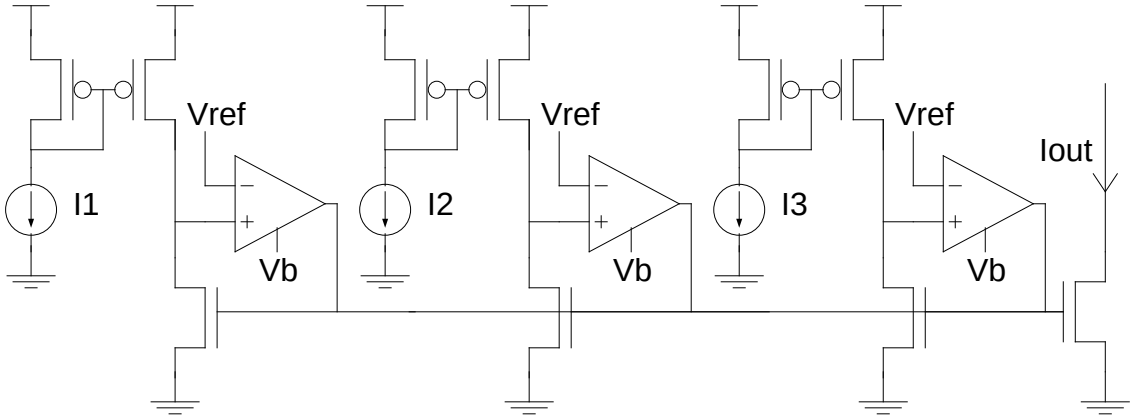
1. (25 points) Solve the following circuit for V_{out} in terms of the inputs and other circuit parameters. Feel free to make any reasonable assumptions but clearly state and justify them. Assume that $\kappa \neq 1$ but is the same for all devices.



2. (25 points) Determine the numerical value of V_{out} for the following circuit for $V_{in} = 0.7V$ and $V_{DD} = 5V$. $I_0 = 3 \times 10^{-21}A$ and $\kappa = 0.7$ for all devices. Feel free to make any reasonable assumptions but clearly state and justify them.



3. (25 points) Answer the following questions for this subthreshold CMOS circuit that performs a useful function. Note that there are three transamps in the circuit and remember that these are current-output devices. Assume that the transamps have no input or output voltage restrictions, $VDD = 5V$, $V_{ref} = 2.5V$ and $\kappa = 1$. Feel free to make any reasonable assumptions but clearly state and justify them.



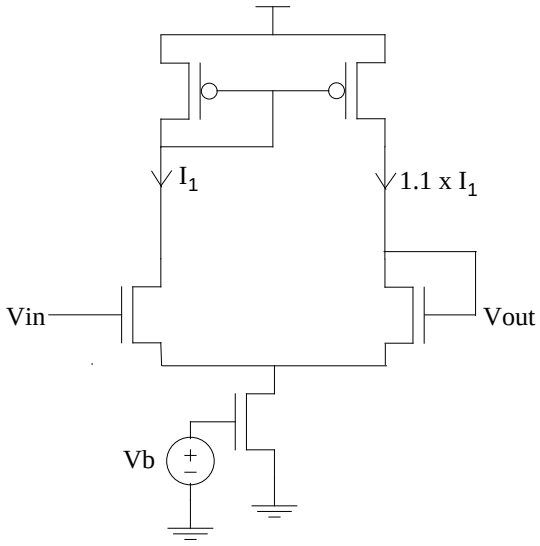
(a) (10 points) What is I_{out} when $I_1 = I_2 = I_3$? Explain.

(b) (10 points) What is I_{out} when $I_1 \gg I_2 \gg I_3$? Explain.

(c) (5 points) What is the function of this circuit? Explain.

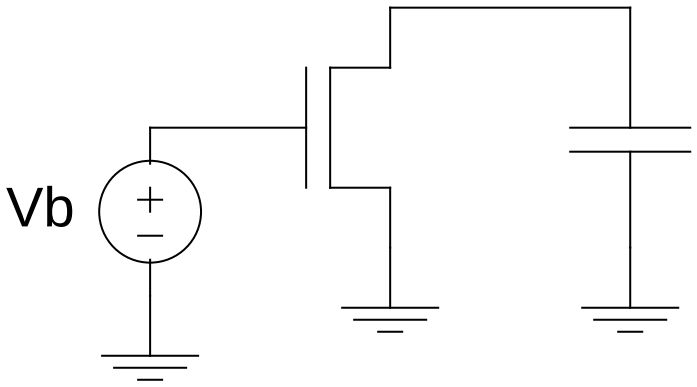
4. (25 points) Short Answer.

   (a) (5 points) For the following circuit, assume that the pfet current mirror is mismatched such that the current output of the mirror is 10% larger than the current input. This is the only nonideality in the circuit, the differential pair is perfectly matched and all transistors have infinite output impedance. Assume that $\kappa = .7$ for all devices. For sub-threshold operation, what is the numerical value of the voltage offset of the transamp? In other words, what is the numerical value of $V_{out} - V_{in}$ in Volts?



   (b) (5 points) Consider two nfets in a standard CMOS process. Is it possible for them to be drawing the same amount of current yet one of the transistors is in the subthreshold region while the other is in the above threshold region? Explain.

(c) (5 points) How long will it take for a MOS transistor drawing 1nA of current to discharge a 1 pF capacitor? $V_b = 0.7V$ and $\kappa = 0.7$ Assume that the capacitor must be discharged from 5V to 100mV.



(d) (5 points) As discussed in class the resting potential of the cell membrane of a biological neuron is about -70mV while the potential of the extracellular fluid is ground. When an action potential is initiated, Na^+ ions flow into the cell to raise its potential well above ground (to about +40mV). In order to increase the cell potential above ground, Na^+ ions must flow against the voltage gradient, from the grounded extracellular fluid into the positively charged cell membrane. How is this possible? Explain.

(e) (5 points) A student proposed an alternative silicon neuron that uses a pfet instead of a capacitor to implement the positive feedback mechanism required for the action potential. Her circuit is shown below. When the inverter threshold is reached, the first inverter flips and its high output turns on the pfet which rapidly charges the capacitor to Vdd. Discuss the fundamental problem with this neuron circuit.