EEL 6935: HW#4

Due Wednesday, November 27, 2002 at midnight. Late homework loses $e^{\#\ of\ days\ late} - 1$ percentage points. See the current late penalty at http://www.cnel.ufl.edu/hybrid/harris/latepoints.html

This homework is pass/fail, you must complete all of the steps to pass. The goal of this homework is layout and verify a full chip including the padframe in the 0.6um AMI process. If you are having trouble with this assignment, come to the ECEL lab at 3-4pm on Tuesday, Nov 26 (Vishnu) or during class time 12:50-1:40pm on Wednesday, Nov 27 (Du) for additional help. There will be no class on Wednesday, Nov 27.

You will use your transamp layout from HW#3 and produce a chip suitable for fabrication. All pad inputs that go solely to gates should be wired to PadIO pads. The current output from the transamp should be wired to an ARef pad. You can read a complete description of the pads at http://www.mosis.org/cell-libraries/scn05-pads-tiny/mAMI05P.pdf This is a 53-page color document that you should think twice about printing it out.

You can implement your chip in whatever layout system you like as long as you can run the DRC and LVS on the entire chip. If you use CADENCE, follow the following detailed steps:

1. Make sure that your transamp layout from HW#3 passes the DRC and LVS with no problems

2. Copy the padframe files on the ECEL computers with the following command: "cp -r ~chend/PadFrame ." This command will create a PadFrame subdirectoy in whichever directory you run the command from. If you do not have an account on the ECEL system, contact duchen@cnel.ufl.edu for details of how to obtain the padframe.

3. Once the PadFrame directory is copied, it needs to be added to the library path for the CADENCE library manager to access it. To do this, you should go to the ICFB main window, TOOLS->Library Path Editor and add "PadFrame" as library and "./PadFrame" as Path (without the quotes). Then save the library path.

4. Observe the layout and the schematic of the padframe with Cadence.

5. Perform the LVS of the padframe and make sure that there are no LVS errors. Note that there are design rule errors in the padframe so no need to run the DRC just yet.
6. While in the layout view:
   (a) Place your transamp inside the padframe
   (b) Swap in the correct pads into the padframe as needed (remember PadIO to input signals that only go to gates)
   (c) Wire up the signal and power lines from the transamp to the padframe
   (d) Run the DRC for the whole chip ignoring errors within the padframe.
   (e) Extract the entire layout to a netlist
7. While in the schematic view:
   (a) Change the padframe schematic to reflect the changes that were made in the padframe. Make sure to change the padname and signal names to match the old pads that were deleted.
   (b) Combine the padframe and transamp schematics into one view
   (c) Wire up the signal and power lines between the padframe and the transamp
8. Run LVS to verify the whole chip. This should create a file called si.out in your LVS subdirectory.
9. Export the chip to a cif file. EXPORT can be reached from the ICFB main window with ICFB->File->Export->CIF The file name should be

   `firstname_lastname.cif`

   in lowercase letters so, for example, your instructor's filename would be called

   `john_harris.cif`

What to hand in: Email the two file attachments (the correct cif file and the si.out file citing no errors) to xinqi@cnel.ufl.edu Also report in the body of the message any problems that you encountered during the assignment (if any). You should not hand in any hardcopy.

Since it is highly improbable that two students could independently generate exactly the same cif file, any two cif files that are exact copies of one another will result in failing grades for the assignment.