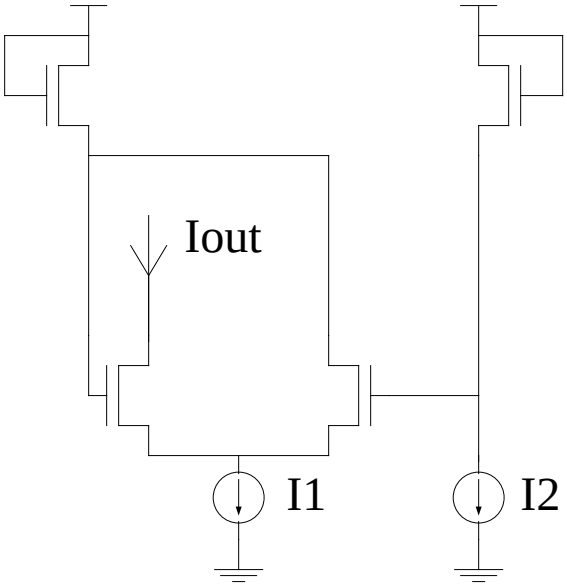
EEL 6935: HW#2

Due Friday, September 27, 2002 in class. Late homework loses $e^{\#\ of\ days\ late} - 1$ percentage points. See the current late penalty at http://www.cnel.ufl.edu/hybrid/harris/latepoints.html

1. Solve for I_{out} as a function of I_1 and I_2. As usual, first, assume $\kappa = 1$ and derive your answer. Then assume κ is the same for all transistors but not equal to one and derive your answer. Show all of your work and explicitly state all assumptions, e.g. which transistors are in saturation, subthreshold operation, matching of devices, etc. You will have to think a little bit more about this circuit than those in HW#1.



2. Derive another expression for the output voltage limitation of the five-transistor transconductance amplifier using the following constraint. Assume that the value of V_{out} is valid until it changes the output current by I_B from its nominal value. Give a simplified rule of thumb for the limits of V_{out} and, as usual, state all of your assumptions.

For the final questions, you must have access to a circuit simulator. Examples include CADENCE SPECTRE, PSPICE, HSPICE, and winspice but use whichever simulator you feel comfortable with. Note that winspice is shareware that is available from www.winspice.com. We will be using the 0.6um AMI process available through MOSIS. Complete information about the process is available through
http://www.mosis.org/Technical/Processes/proc-ami-c5n.html
UF CADENCE users will already have this process available but other simulators may require the following model files available at
http://www.cnel.ufl.edu/hybrid/courses/EEL6935/nmos.txt
and
http://www.cnel.ufl.edu/hybrid/courses/EEL6935/pmos.txt

3. For a 6um x 6um nfet transistor, plot the Ids vs. Vgs curve for the device. Calculate the approximate value of κ. Completely describe how you performed the calculation. Also, come up with a rule for defining what the threshold of the transistor is.

4. For a 6um x 6um nfet transistor, plot the Ids vs. Vds curve for the device. Calculate the approximate value of the Early Voltage V_E. Completely describe how you performed the calculation. Also, come up with a rule for defining what the saturation voltage is.

5. Verify your solution of Problem 1 for I_{out} as a function of I_1 and I_2. Show plots and compare your theoretical solution to the simulation.

6. Verify the output voltage limitation of the transamp that you discussed in Problem 2. How accurate are your limits on V_{out} for a variety of V_1 and V_2 values?