A CMOS NEURAL OSCILLATOR USING NEGATIVE RESISTANCE

Han Jung Song, John G. Harris*

Dept. of Electronic Engineering, Chung Cheong College, Chung-Buk 363-890, Korea
*Dept. of Electrical & Computer Engineering, University of Florida, Gainesville, FL 32611, USA
E-mail : hjsong@ok.ac.kr, harris@cnel.ufl.edu

ABSTRACT

A CMOS neural oscillator using negative resistance has been designed and fabricated in an AMI 0.5um double poly technology through MOSIS. The proposed neural oscillator consists of a nonlinear resistor with negative resistance as well as standard OTAs and capacitors. Simulations of a network of oscillators demonstrate cooperative computation. Measurements of the fabricated oscillator chip confirm the input-gated oscillatory behavior of the cell.

1. INTRODUCTION

Many researchers believe that neural oscillations are triggered by sensory stimulation and that these oscillations are used in subsequent computation. The simplest models hold that synchronous oscillations occur across an extended brain region if the stimulus constitutes a coherent object. A recent example of this type of model is Terman and Wang's LEGION model [1]. More sophisticated models of brain activity, such as Freeman's olfactory model propose chaotic networks of local oscillators for associative memories and other computations [2]. Much research has been done in integrating these and similar oscillatory models into analog VLSI hardware to greatly speedup timeconsuming simulations, e.g. see [3-10]. This paper introduces a very simple coupled neural oscillator using negative resistance and its resulting network computation is demonstrated.

The outline of the paper is as follows: Section 2 describes the ideal coupled oscillator of OTAs and capacitors. Section 3 describes the nonlinear CMOS resistor for neural oscillation. In section 4, we will show complete coupled oscillator and an example of its simple network computation. Section 5 presents experimental measurements and analysis of the fabricated chip. Section 6 is a brief summary.

2. COUPLED OSCILLATOR USING TRANSCONDUCTORS

An ideal coupled oscillator using two operational transconductace amplifiers (OTAs) and two capacitors is shown in Fig. 1.

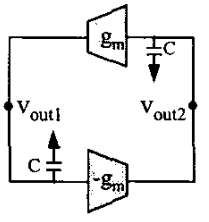

Fig. 1 Ideal coupled oscillator using OTAs and capacitors.

Circuit equations derived from Fig. 1 are given by the following first order differential equations.

$$C\frac{dVout1}{dt} = g_m \cdot Vout2$$
$$C\frac{dVout2}{dt} = -g_m \cdot Vout1 \quad (1)$$

where g_m is the small-signal tranconductance of the OTA, Vout1 and Vout2 are node voltages, and C is the capacitance. High-level MATLAB simulations of equation (1) confirm analytic results predicting convergence to a limit cycle, see Fig. 2(a) for simulation results using C=1 pF, g_m =1 uS. However practical OTAs have nonzero output conductance (g_o), considering output conductance (g_o) of the OTA, equation (1) is modified to equation (2).

$$C\frac{dVout1}{dt} = g_m \cdot Vout2 - g_o \cdot Vout1$$
$$C\frac{dVout2}{dt} = -g_m \cdot Vout1 - g_o \cdot Vout2 \quad (2)$$

For the case of g_o = 50 nS, analysis and MATLAB simulations of equation (2) show that the voltage waveforms converge to a fixed point, shown in Fig 2(b). Detailed SPICE simulations of Fig. 1 lead to the same results and are shown in Fig. 2(c).

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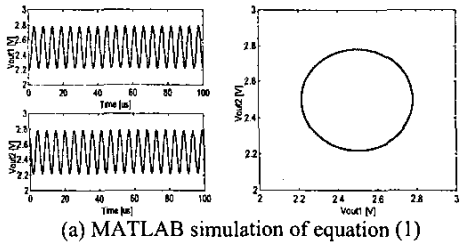
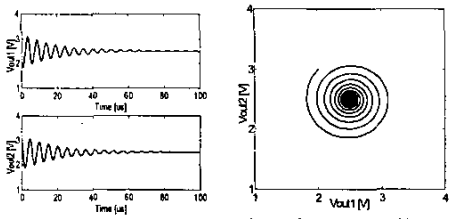
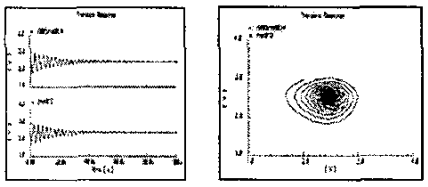


(a) MATLAB simulation of equation (1)



(b) MATLAB simulation of equation (2)



(c) SPICE circuit analysis

Fig. 2 Simulation results of Fig. 1 circuit (time responses and phase plots, reference voltage = 2.5V)

We propose to add explicit negative resistance to overcome the positive output resistance of the OTAs and thereby attain a sustained limit cycle oscillation. The configuration, shown in Fig. 3, uses a negative, nonlinear CMOS resistor as a current supply for compensation of consumed charge through the output conductance.

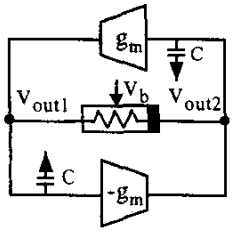


Fig. 3 Coupled oscillator with negative, nonlinear resistor.

3. NONLINEAR CMOS RESISTOR WITH NEGATIVE RESISTANCE

Fig. 4 is the proposed nonlinear CMOS resistor with negative resistance. This circuit consists of an OTA and a bump circuit with bias voltage Vb [10]. The bump circuit block is a nonlinear resistor whose conductance is a Gaussian-like function of the difference of the input voltages. Its simulated I-V curve is shown in Fig. 5. Current from the bump circuit is used as the bias current of the positive feedback OTA. A diode-connected MOS transistor and a capacitor can be used as a summing node as shown in the figure. Fig. 12 shows the measured I-V curve of the resulting resistor showing negative resistance that decreases to zero as the voltage drop increases.

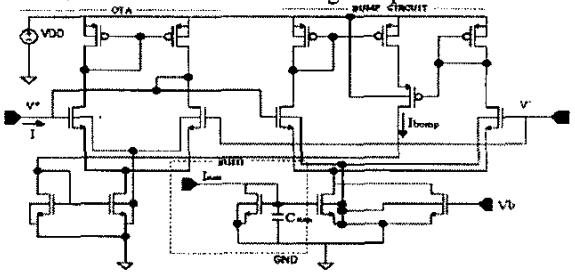


Fig. 4 Proposed nonlinear CMOS resistor.

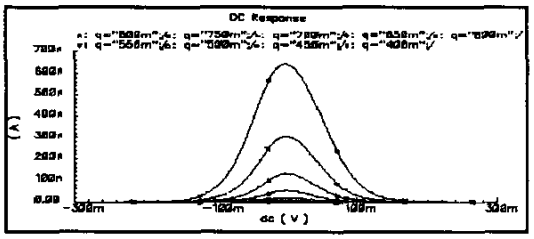


Fig. 5 SPICE simulated I-V curve of the bump circuit block in Fig. 4

4. CMOS COUPLED NEURAL OSCILLATOR AND ITS SIMPLE NETWORK APPLICATION

The complete schematic of the proposed neural oscillator is shown in Fig. 6. For faster convergence of the neural oscillator, another negative feedback OTA is added.

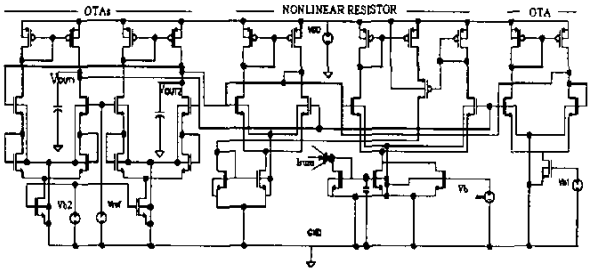
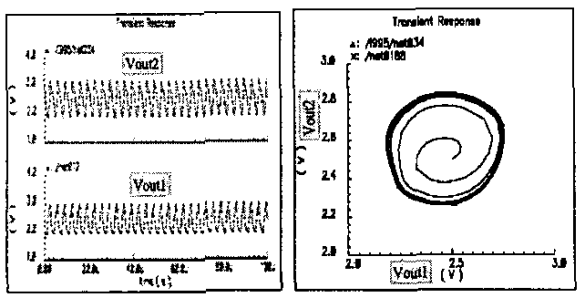


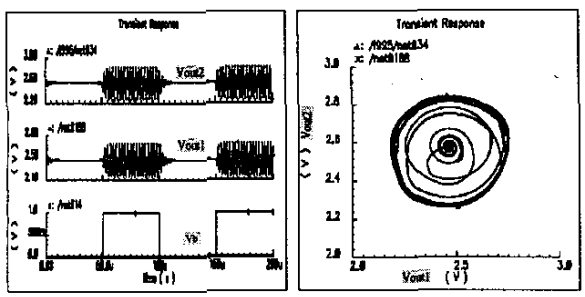
Fig. 6 Schematic of the proposed coupled CMOS neural oscillator.

The external bias voltage Vb determines whether the circuit oscillates or not. This node can be used to sum the influence (as currents) of other oscillators. If the sum of the currents at this node is greater than a certain threshold, a firing sequence of pulses is generated. If the sum of currents is below the threshold, the cell converges to a

fixed point. SPICE analysis of the oscillator, shown in Fig. 7, shows that the proposed circuit generates oscillating signals in response to specific bias voltage.



(a) time responses and phase plot of DC input (Vb = 0.8[V])



(b) time responses and phase plot of the square wave input

Fig. 7 SPICE simulation results of the proposed neural oscillator (in condition of 2.5 V reference)

The synapses between neural oscillators are made with wide-range OTA[12] with current sources or sinks. The weight of each synapse can be adjusted by changing the g_m of the OTA. Fig. 8 shows the synapse schematic of the proposed neural oscillator. Excitatory synapses use an output current that is a positive half-wave rectified version of the input voltage. In case of inhibitory synapse, the output is a negative half-wave rectified current [12].

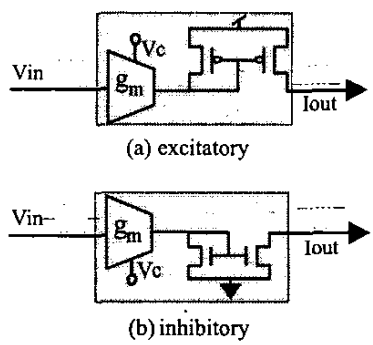


Fig. 8 Synapse circuits of the proposed neural oscillator.

Fig. 9 shows a simple network with excitatory and inhibitory connections between oscillators. As external stimulus, half-overlapped 10 kHz square wave pulses (50% duty cycle) are applied to Vb1 and Vb2, respectively.

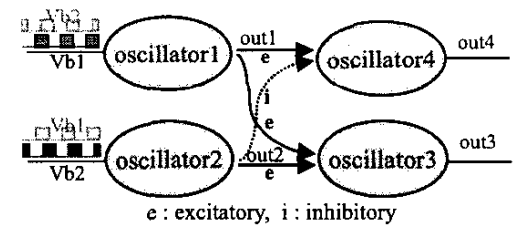


Fig. 9 Simple networks with excitatory and inhibitory.

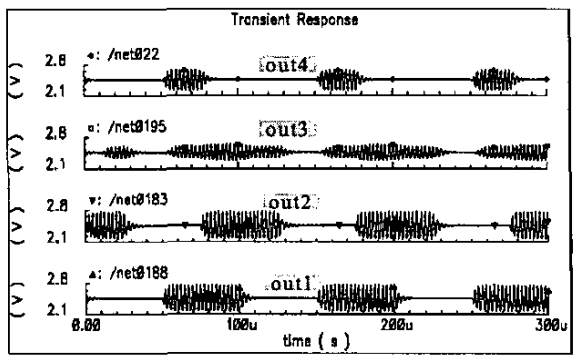


Fig. 10 SPICE simulation results of the network in Fig. 8

From Fig. 10, out1 and out2 are the outputs of oscillator1 and 2, respectively which oscillate only when their respective inputs are high. The output (out3) of oscillator3 with all excitatory connections is shown to oscillate when either out1 or out2 oscillate. The output (out4) of oscillator4 with a excitatory and a inhibitory connection only oscillates with out1 oscillates and out2 does not.

5. MEASUREMENT AND ANALYSIS OF THE FABRICATED COUPLED NEURAL OSCILLATOR

Fig. 11 shows a microphotograph of the neural oscillator chip, which is fabricated by using the AMI 0.5um double poly double metal CMOS technology.

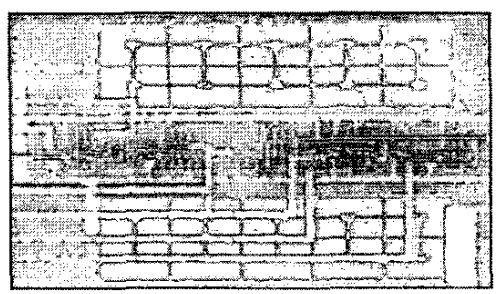


Fig. 11 Microphotograph of the fabricated neural oscillator.

Pins of the chip include power supply terminals (Vss, V_{DD}), output voltage terminals (Vout1, Vout2), and the bias terminal of the nonlinear resistor Vb. I-V curves of the nonlinear CMOS resistor according to bias voltage Vb (05 V ~ 0.7 V) are shown in Fig. 12.

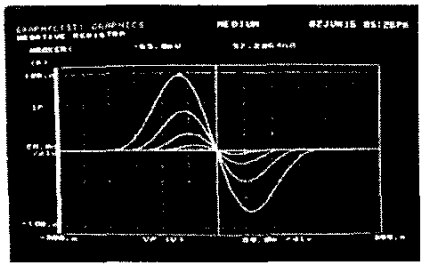
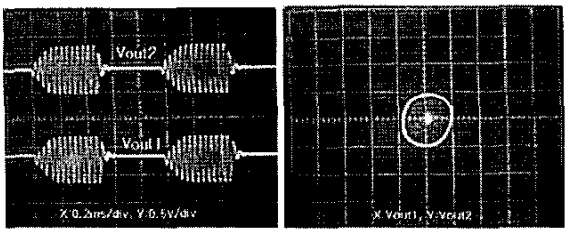
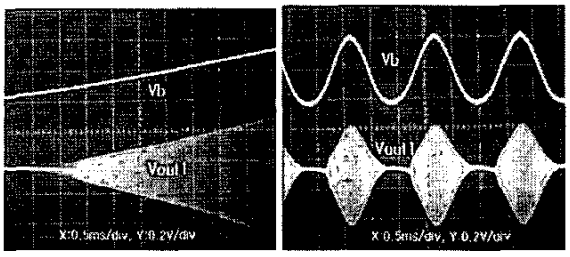


Fig. 12 Measured I-V curves of the nonlinear negative CMOS resistor according to bias voltage Vb.

As shown in the figure, in the vicinity of the center, there are negative resistance regions. Fig. 13 (a) illustrate time responses and phase plot of the oscillator for 1kHz square wave Vb (duty cycle=50%). As shown in the figure, oscillation occurs in case of high Vb. Similarly, In figure 13 (b) and (c), the circuit oscillates in a sinusoidal fashion when the input Vb exceeds a certain threshold level. Similar results are obtained for the KII circuitry implementing Freeman's olfactory model but requires much more complicated circuitry [8].



(a) time responses and phase plot in pulse input



(b) time responses in linear and sine wave input

Fig. 13 Measured data of the neural oscillator

6. CONCLUSION

In this paper, a coupled neural oscillator using a nonlinear, negative resistor is designed, simulated and implemented in a 0.5um double poly CMOS process. Simple network performance is demonstrated through simulations and measured data is shown for a single fabricated oscillatory cell.

ACKNOWLEDGMENTS

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