A Continuous-Time Analog Circuit for Computing Time Delays Between Signals

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Abstract—
We describe an analog VLSI circuit that computes the time delay between an arbitrary input signal and its delayed version. Versions of this circuit will be used as the basic computational elements for human auditory localization models in both the horizontal and vertical directions. Since the circuit uses subthreshold CMOS circuitry, chip measurements show that delays ranging over five orders of magnitude can be recovered. The circuit delays the first input signal by two distinct time-constants and correlates each with the second input signal. The correlation values at the two points are then integrated and used to compute a finite-difference derivative that dynamically adjusts the time constants until an optimal delay is found. This paper describes the first continuous-time circuit for computing delays between arbitrary signals.

I. Introduction

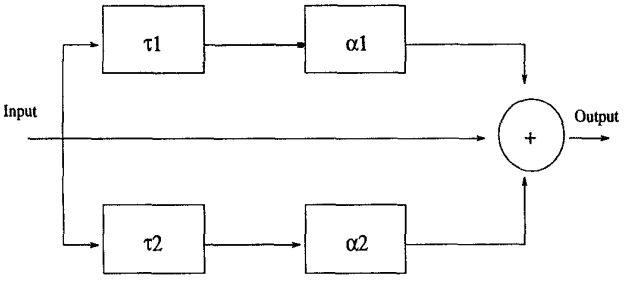

Fig. 1. *Delay and add model.*

Sound localization in humans requires explicit measurement of time delays. The primary cue for localization in the horizontal direction is the interaural time difference. Localization in the vertical direction is much less understood, but researchers believe that spectrum shape is the primary cue for vertical sound localization [2] [8] [3]. The nature of the spectrum shape provides constraints for processing in the time domain. For example, the time domain model proposed by Batteau [1] successfully maps elevation angles to time delays in certain regions through psychoacoustic experiments. Batteau concluded that the physical structure of the external ear introduced two significant echoes in addition to the original sound. This model, shown in Figure 1, relates the output $y(t)$ with the input $x(t)$ as:

$$y(t) = x(t) + \alpha_1 x(t + \tau_1) + \alpha_2 x(t + \tau_2) \qquad (1)$$

where τ_1 refers to the azimuthal echo and τ_2 refers to the elevation echo; α_1 and α_2 are the two constants representing

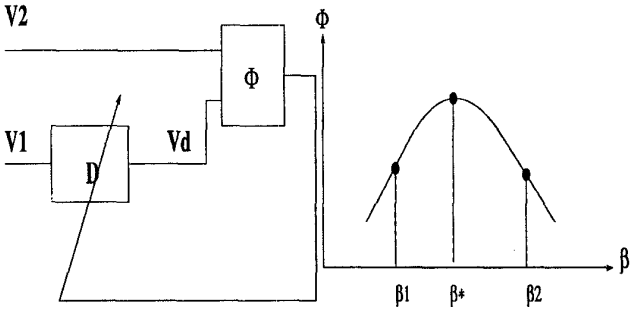

Fig. 2. *(a)Block diagram of the algorithm (3). (b)The computation of the maximum value.*

the corresponding reflection coefficients. This time domain model is called the delay-and-add model. When τ_1 is fixed at some value in the range of 0 to 80μs and τ_2 is varied from 120μs to 260μs, the sound source is perceived from 60 to -40 degrees with 0 degree defined to be the same horizontal plane as the two ears. [9]. The advantage of the delay-and-add model is its simplicity and its natural physical basis. Since delays must be measured for both horizontal and vertical sound localization, our goal is to design a system which can trace the signal's phase delay in continuous time. As a first step, we describe a simple circuit that computes the delay between two input signals by adapting the delay through a delay element to match the temporal disparity of the signals. The bias voltage will be adaptive to control the delay through the delay elements. Lazzaro has demonstrated a delay computation circuit using finite delays of pulsed signals [5] and more recently Liu has developed an adaptive delay system using discrete-level signals [6]. The circuit described in this paper operates on arbitrary input signals in continuous-time.

II. Algorithmic Solution

Assume that the system is presented an original signal $f(t)$ and its delayed version $f(t + \alpha)$. We also assume that $f(t)$ is the output of one tap of a silicon cochlea or has been otherwise bandpass filtered. The system must determine the value of the delay α. The algorithm first delays the original signal $f(t)$ by some delay β creating $f(t + \beta)$. This signal is then correlated with the original delayed signal $f(t + \alpha)$ and integrated. If we define the correlation function as $\phi()$ then the goal is to find the value

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of β that maximizes the following relation:

$$\max_{\beta} \int \phi(f(t+\alpha), f(t+\beta))dt = \max_{\beta} \Phi(\beta) \qquad (2)$$

Several schemes could be used to find the value of β that optimizes the correlation. These methods include:

1. Search all possible values of β and keeping the value that results in the largest signal correlation. This method is time-intensive.
2. Build many delay circuits in parallel, each using a different value of β. This method is hardware intensive.
3. Dynamically adjust the delay of a single delay circuit until a locally optimal value is discovered. The control algorithm requires the computation of $\partial\Phi/\partial\beta$ which is problematic.

We chose to implement algorithm 3. The block diagram of this algorithm is illustrated in Figure 2. If the initial point is at β_1, the derivative of the Φ represents the slope of the tangent line at the point of β_1. The derivative provides the information regarding the direction of changing β to reach the maximum value of the Φ function. The change of the β value is:

$$\Delta\beta = \mu(\partial\Phi/\partial\beta) \qquad (3)$$

μ is some constant. If on the other hand the initial value is at β_2, the derivative of the Φ is negative. Thus, the direction of changing β is on the other direction. The maximum value of the Φ function is located at β^*. To estimate the time of reaching the maximum Φ function from the initial point β_1, we can derive the following equation by simply assuming the $\partial\Phi/\partial\beta$ is a constant.

$$\Delta t = (\beta_* - \beta_1)/\mu * (\partial\Phi/\partial\beta) \qquad (4)$$

This equation shows the time to reach the maximum value of the Φ function depends on the initial point, and the value of $\partial\Phi/\partial\beta$. The assumption made to derive the above equation is not exactly correct. Since the value of $\partial\Phi/\partial\beta$ is smaller at the points which are closer to the final point β_* compared to the initial point β_1.

We have chosen a compromise solution for our implementation in which two delay circuits are used with two slightly different time delays. This allows a two-point finite difference approximation to the derivative $\partial\Phi/\partial\beta$ using the correlation values from the outputs of the two delay circuits. The choices for the $\phi(x,y)$ include xy, $-|x-y|$ and other norms. To simplify the implementation, we have chosen the bump function that arises from the bump circuit developed by Delbruck [4]. The bump circuit gives a ϕ function of the form:

$$\phi(x,y) = \frac{I_b}{2} \frac{1}{\cosh^2((x-y)/2V_T)} \qquad (5)$$

where I_b and V_T are constants.

The block diagram of the phase detector is shown in Figure 3. This system includes two delay elements, two bump circuits, a comparator, and a capacitor which is used to

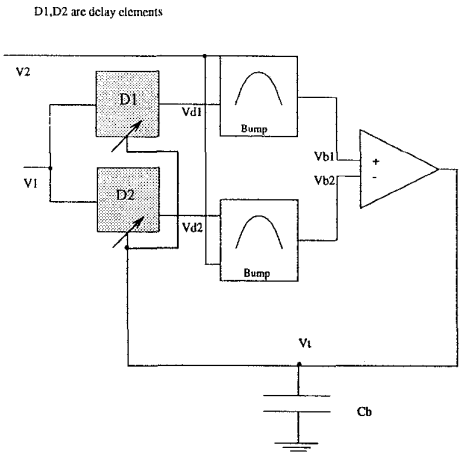

Fig. 3. *Block diagram of the phase detector.*

store the bias voltage of the delay elements. The bias voltage, which allows monotonic adaptation, controls the delay. These circuits are all operated in the subthreshold region using CMOS transistors. In Figure 2, two input signals, V_1 and V_2, are fed into the system. Assuming both signals have the same amplitude and frequency, but different phase delays, the input signal V_1 goes to two delay elements D1 and D2. Each delay element gives the d1 and d2 delay respectively. The outputs of D1 and D2 are called V_{d1} and V_{d2} respectively. Our goal is to adaptively control the d1 and d2 phases to make the phase of V_{d1} and V_{d2} approach the phase of the other input signal V_2. The bias voltage of the delay elements would then encode the phase delay of the V_2. The fundamental correlation element for the temporal disparity computation uses the bump circuit [4]. Two bump circuits compare V_2 vs. V_{d1} and V_2 vs V_{d2}, to make the computation. The outputs of the two bump circuits are called V_{b1} and V_{b2}. The purpose of using two bump circuits is to provide relative difference information of V_2 vs V_{d1} and V_2 vs V_{d2} for the system. The capacitor will be charged or discharged from the information. Simplifying the implementation details slightly, assume d1 is set to be twice d2. We will have three cases to discuss: (i) V_{b1}=V_{b2} implies that V_{d1} and V_{d2} produce the same correlation with V_2 and the system stablizes. (ii) $V_{b1} > V_{b2}$, that is V_{d1} (the longer delay) correlates better with V_2. Since d1 is two times d2, the delays should be increased. This is accomplished by decreasing Vt. (iii) $V_{b1} < V_{b2}$ means that the shorter delay correlates better with V_2. The delays should be decreased which is accomplished by increasing Vt. In conditions (ii) and (iii), the comparator drives the voltage on the capacitor until the bump circuits report an equal correlation, i.e. condition (i). The resulting voltage on the capacitor encodes the delay between the two input signals.

III. Hardware Implementation

The delay block has been implemented using an all-pass filter which gives a gain of one over all frequencies but adds a frequency dependent phase delay. The difference

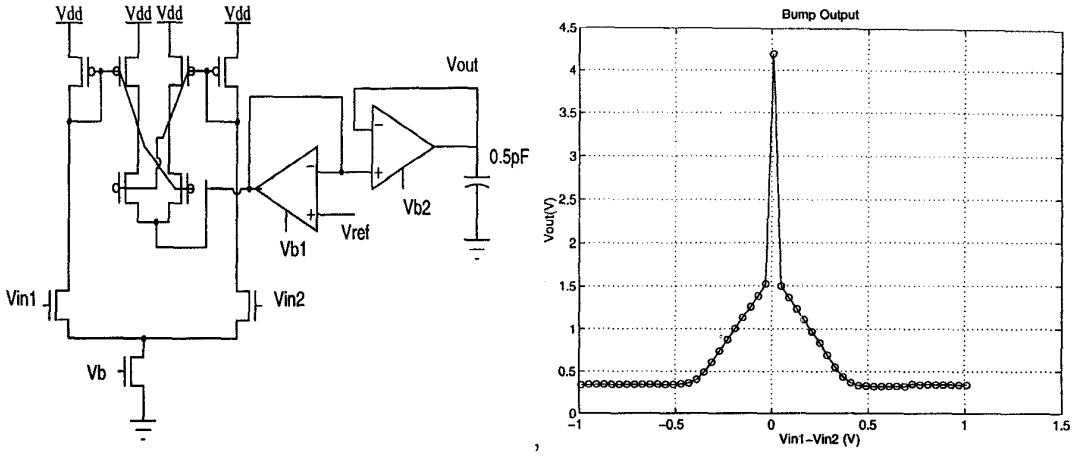

Fig. 5. *(a)Bump circuit diagram. (b)Measured data from the fabricated bump circuit.*

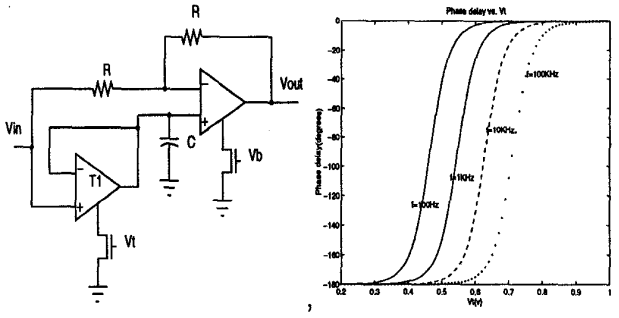

Fig. 4. *(a)All pass filter schematic implementation. (b)The phase delay characteristics.*

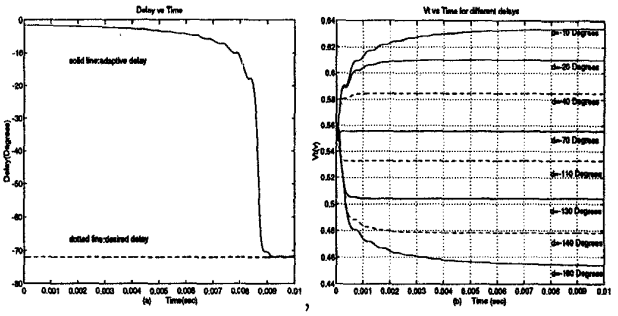

Fig. 6. *(a) SPICE simulation for the circuit computing a phase delay of 72 degrees at 1KHz. (b) SPICE simulation for computing various delays starting from a common initial starting point, 0.55V.*

between this circuit and a standard phase shifter is that the bias voltage is adaptive.

A block diagram for the all-pass circuit is shown in Figure 4(a). All components are implemented using subthreshold building blocks described by Mead [7]. The resistors (R) are implemented using simple transamp followers. The transfer function of the filter is:

$$\theta = -2\arctan(\frac{f}{f_0}) \tag{6}$$

where f is the signal's frequency, and f_0 is the resonant frequency of the phase shifter given by

$$f_0 = \frac{\kappa I_0 e^{(\frac{\kappa V_t}{V_T})}}{4\pi C V_T} \tag{7}$$

where κ is a processing constant, and V_T is the thermal voltage. In the range, $0.1 \leq \frac{f}{f_0} \leq 10$, phase varies approximately linearly from 0 to 180 degrees. The phase shifter output is a function of the signal's frequency. The relation of the V_t vs. phase delay for different frequencies is shown in Figure 4(b). For higher signal frequencies, the curves are shifted to the right. Simulated phase delay characteristics are shown in Figure 4(b). The fabricated circuit has a subthreshold bias (V_t) that control the effective 3db point from as low as a few Hz to 40KHz.

The bump circuit is shown in Figure 5(a). V_{in1} and V_{in2} are two inputs of the bump circuit. The bump circuit works as the function of Φ we described in the algorithm. The correlation values of the two input signals, V_{in1} and V_{in2} are then integrated to the value of V_{out}. The measured data from the chip is shown in Figure 5(b).

We have designed and tested a $2\mu m$ CMOS circuit that implements the phase detector. Figure 6(a) shows a SPICE simulation for the circuit computing a phase delay of 72 degrees in 10ms. Figure 6(b) shows another SPICE result for computing various delays starting from a common initial starting point. Since the circuit encodes the logarithm of delay as a voltage, delays ranging over five orders of magnitude can be recovered.

The measured data from the fabricated chip is shown in Figure 7. This figure shows the phase delay vs V_t for different frequency signals. We use two sinusoidal waves with a certain phase difference as the two input signals V_1 and V_2. From the test, we observe the output voltage V_t has linear mapping relation with phase delay in the range from -10 to -170 degrees. The three curves are for frequencies which are equal to 10, 100, and even 10kHz.

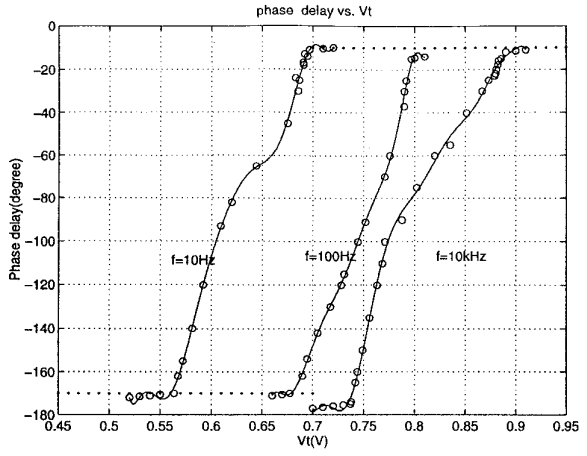

Fig. 7. *Measured from the fabricated chip showing the phase delay vs voltage Vt for signals with 3 different frequencies.*

IV. Conclusion

We have described the first continuous-time circuit for computing delays between arbitrary signals. Modified versions of this circuit will be used as the basic computational elements for human auditory localization in both the horizontal and vertical directions. The phase detector chip has been completely designed, simulated, fabricated and tested.

Acknowledgements

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